MODEL: ST2151B03-2

Ver. 2.1

Date: 06.Dec.2018

Customer's Approval	CSOT
Signature Date	Approved By Product Director Date Name: Stefan Chen Signature:
	Reviewed By PM Manager Date Name: Xiuyi Wang Signature:
	Reviewed By Project Leader Date Name: Wei Li Signature:
	Reviewed By PM Date Name: Louis Xu Signature:

1. General Description

1.1 Product Features

- **FHD Resolution (1920 * 1080)**
- **High Brightness: 1000 cd/m2**
- **Very High Contrast Ratio: 4000:1**
- **Low Power Consumption: Typ. 27.6 W**
- **Fast Response Time:6.5ms**
- **High Color Saturation: 72% NTSC**
- **Ultra Wide Viewing Angle: 178°(H)/178°(V) (CR≥10)**
- **DE (Data Enable)Mode**
- **LVDS (Low Voltage Differential Signaling) Interface**

1.2 Overview

ST2151B03-2 is a diagonal 21.5" color active matrix LCD open cell with 2ch-LVDS interface. This open cell is a transmissive type display operating in the normally black mode. It supports 1920 * 1080 FHD resolution and can display up to 16.7M colors (8bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe.

This open cell dedicates for LCD TV & Monitor products and provides excellent performance which includes high brightness, ultra wide viewing angle, high color saturation and high color depth. CSOT open cell comply with RoHS for identification.

1.3 General Information

Item	Specification	Unit	Note
Active Area	476.64 (H) x 268.11(V)	mm	
Bezel Opening Area	479.8 (H) x 271.3(V)	mm	
Outline Dimension	495.6 (H) x 292.2(V) x 10.35 (D)	mm	D: From Bezel to Rear
Weight	1.9	kg	Max.
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1920 x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.08275 (H) x 0.24825 (V)	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8bit
Display Mode	Transmissive Mode, Normally Black	-	
Surface Treatment	Anti-glare, Haze 2%,Hard Coating (3H)	-	
Luminance of White	1000	cd/m2	Center Point, Typ.

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings (T_A = 25 ± 2 °C)

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit
		Min.	Max.	
Power Supply Voltage	V_{CC}	-0.3	5.5	V
Input Signal Voltage	V_{IN}	-0.3	3.6	V

2.2 Environment Requirement (Based on CSOT's BLU)

(1) Temperature and relative humidity range are shown as below.

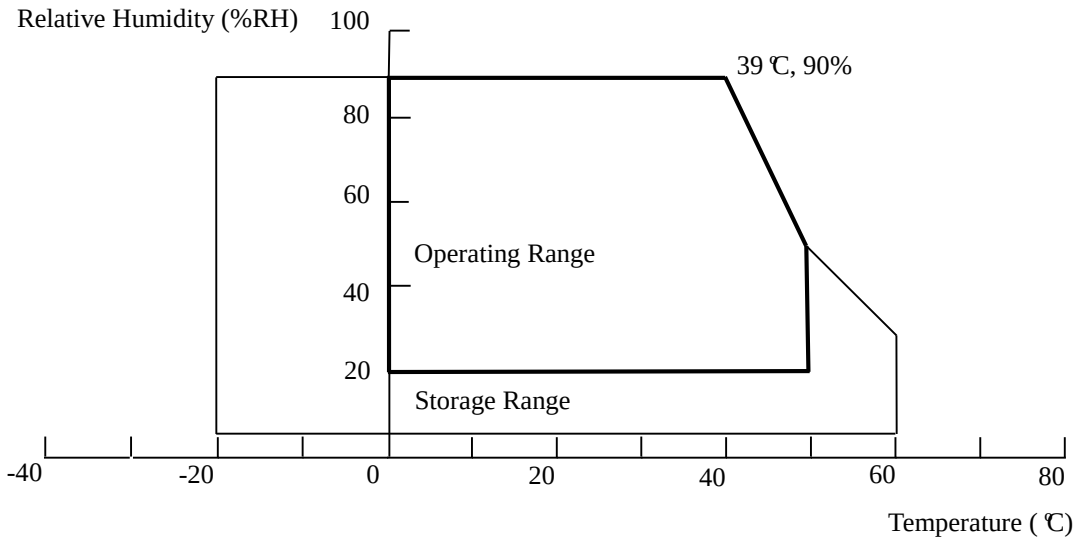


Fig. 2.1 Operating and storage environment

(a) 90%RH maximum ($T_A \leq$ 39 ℃).

(b) Wet-bulb temperature should be 39℃ maximum ($T_A >$ 39 ℃).

(c) No condensation.

(2) The storage temperature is between - 20 ℃ to 60 ℃, and the operating ambient temperature is between 0 ℃ to 50 ℃

The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65℃ with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65℃. The range of operating temperature may degrade in case of improper thermal management in the end product design.

(3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.3 Absolute Ratings of Environment (Open Cell)

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the module in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from 20℃ to 30℃ in normal humidity (50 ±10%RH) with shipping package.

(2) The open cell should be keep within one month shelf life.

3. Electrical Specifications

3.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5	5.5	V	(1)
Rush Current		I_{RUSH}	-	-	1.91	A	(2)
Power Supply Current(@60Hz)	White Pattern	I_{CC}	-	0.89	1.16	A	(3)
	Horizontal Stripe	I_{CC}	-	1.12	1.46	A	
	Black Pattern	I_{CC}	-	0.77	1.0	A	
Power Supply Current(@75Hz)	White Pattern	I_{CC}	-	0.95	1.24	A	(3)
	Horizontal Stripe	I_{CC}	-	1.24	1.61	A	
	Black Pattern	I_{CC}	-	0.79	1.03	A	

Note:

(1) The ripple voltage should be controlled less than 10% of V_{CC}.

(2) Measurement condition: V_{CC} =5V, Rising time = 470μs.

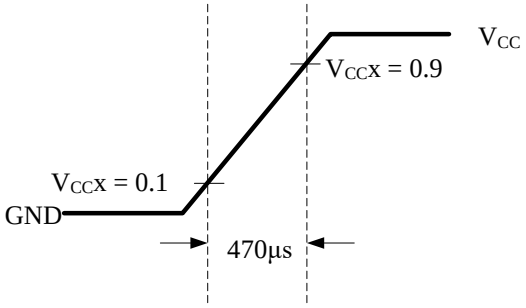
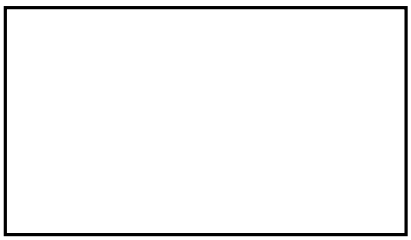


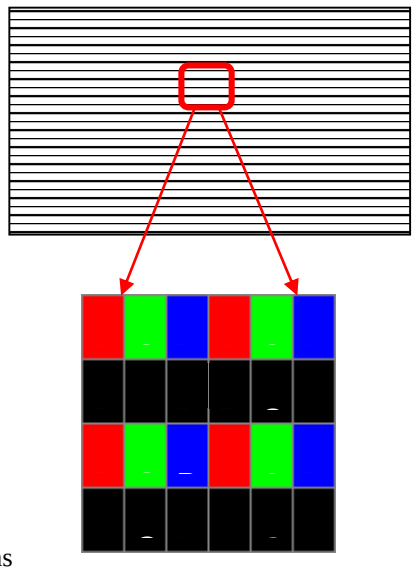
Fig. 3.1 V_{CC} rising time condition

(3) Measurement condition: V_{CC} = 5V, Ta = 25 ±2 ℃. The test patterns are shown as below.

A. White Pattern



B. Horizontal Pattern



C. Black Pattern

Fig. 3.2 Test patterns

3.2 LVDS Characteristics

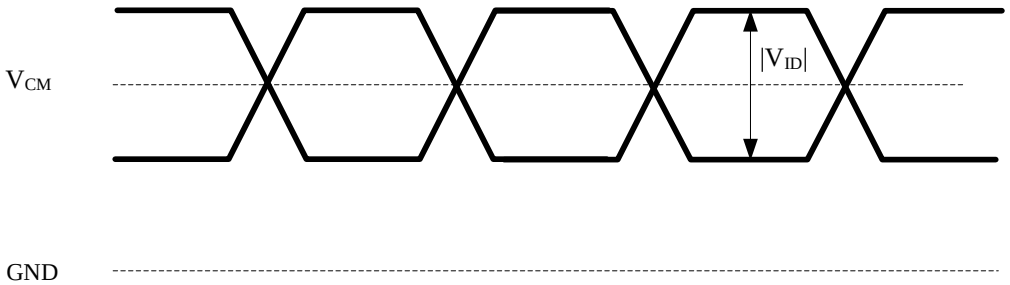
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential Input Voltage	$\|V_{ID}\|$	100	-	600	mV	
	Terminating Resistor	R_T	87.5	100	112.5	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note:

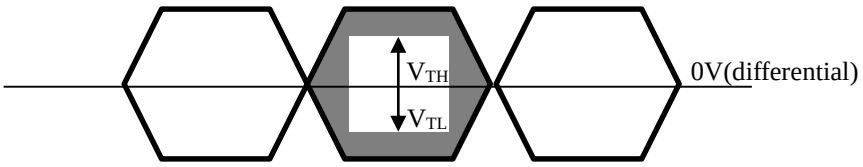
(1) The product should be always operated within above ranges.

(2) The LVDS input signal has been defined as follows:

Single end Signals



Differential Signal



3.3 Temperature Specifications

Parameter	Symbol	Specification			Unit	Recommend test pattern	Note
		Min.	Typ.	Max.			
Surface Temperature	T_{TCON}	–	–	105	℃	Horizontal Pattern	(1)
	T_{Driver}	–	–	115		Horizontal Pattern	(1)

Note:

(1) Any point on the IC surface must be less than Max. specification under any condition ,If the surface temperature is out of the specification, thermal solutions should be applied to avoid be damaged;

3.4 Driver IC ESD Specification

The Electro-Static Discharge tolerance of Source COF IC and Gate COF IC is +-2KV tested by ESD Gun. Especially if the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid be damaged, as shown in Fig.3.4 and Fig.3.5.

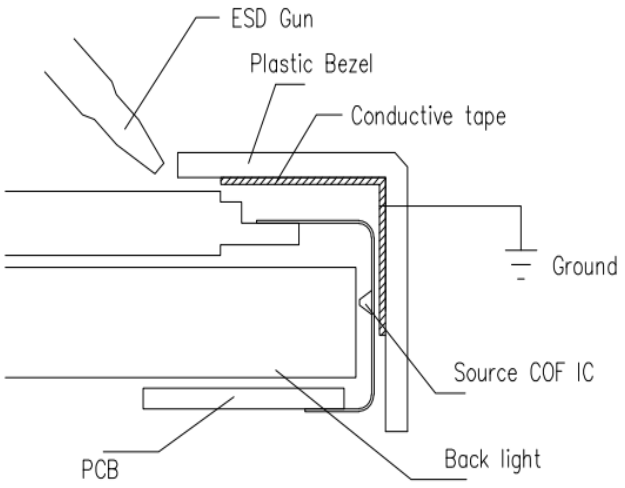


Fig. 3.4 Source COF IC ESD protection

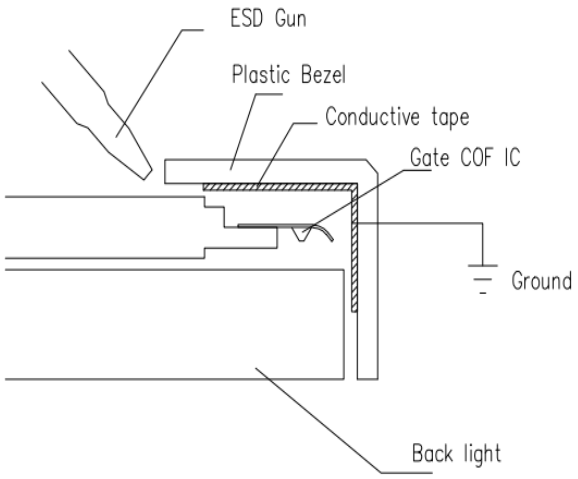


Fig. 3.5 Gate COF IC ESD protection

3.2 Backlight Converter Unit

3.2.1 LED Converter Electrical Characteristics (Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Consumption		$P_{BL(2D)}$		27.6		W_{att}	No dimming
Input Voltage		V_{BL}		12.0		V	
Input Current		$I_{BL(2D)}$		2.3		A	No dimming
		$I_{BL(3D)}$	-	1.25	1.36	A	
Input Inrush Current		I_{RS-VIN}	-	-	5.95	A	(1)
		I_{RS-EN}	-	-	5.95	A	(2)
On/Off Control Voltage	On	V_{BLON}	2.5	3.3	3.6	V	
	Off		0.0	-	0.8	V	
On/Off Control Current	-	I_{BLON}	-	-	1.5	mA	
PWM Dimming Control Voltage	Max.	V_{PDIM}	2.5	3.3	3.6	V	
	Min.		0.0	-	0.8	V	
External PWM Control Current		I_{P-DIM}	-	-	2	mA	
PWM Dimming Frequency		F_{PWM}	140	180	240	Hz	
Dimming Duty Ratio		D_{DIM}	10	-	100	%	(3)
DET Status Signal		DET HI	Open Collector				
		DET Low	0.0		0.8	V	
Input Impedance		R_{IN}	300			Kohm	

Note:

(1) The measurement condition: V_{BL} rising time is 20 ms. (V_{BL} from 10% ~ 90%)

(2) The measurement condition: the V_{BL} = 24V, and then on the V_{BLON} = 3.3V.

(3) Less than 10% dimming control is functional well and no backlight happens to shut down.

4. Input Terminal Pin Assignment

4.1 Interface Pin Assignment

CN1: 300B30-0000RA-M4 (Starconn) or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	RO[0]N	Odd LVDS Signal -	
2	RO[0]P	Odd LVDS Signal +	
3	RO[1]N	Odd LVDS Signal -	
4	RO[1]P	Odd LVDS Signal +	
5	RO[2]N	Odd LVDS Signal -	
6	RO[2]P	Odd LVDS Signal +	
7	GND	Ground	
8	ROCLK-	Odd LVDS Clock -	
9	ROCLK+	Odd LVDS Clock +	
10	RO[3]N	Odd LVDS Signal -	
11	RO[3]P	Odd LVDS Signal +	
12	RE[0]N	Even LVDS Signal -	
13	RE[0]P	Even LVDS Signal +	
14	GND	Ground	
15	RE[1]N	Even LVDS Signal -	
16	RE[1]P	Even LVDS Signal +	
17	GND	Ground	
18	RE[2]N	Even LVDS Signal -	
19	RE[2]P	Even LVDS Signal +	
20	RECLK-	Even LVDS Clock -	
21	RECLK+	Even LVDS Clock +	
22	RE[3]N	Even LVDS Signal -	
23	RE[3]P	Even LVDS Signal +	
24	GND	Ground	
25	WP	Write Protect (High: Write Enable, Low or Open: Write Disable)	(2)
26	SCL	I2C Serial Clock (for adjust VCOM)	(2)
27	SDA	I2C Serial Data (for adjust VCOM)	(2)
28	5V	DC power supply	
29	5V	DC power supply	
30	5V	DC power supply	

Note:

(1)The direction of pin assignment is shown as below:

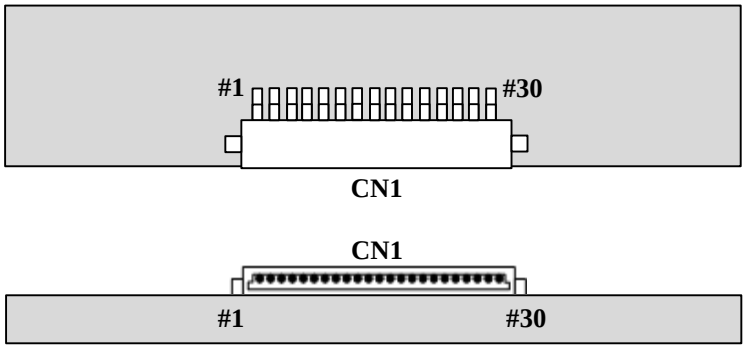


Fig. 4.1 LVDS connector direction sketch map

(2) a. Please let it open (Do not line out from PCBA connector) if it do not used.(for example：TV set)

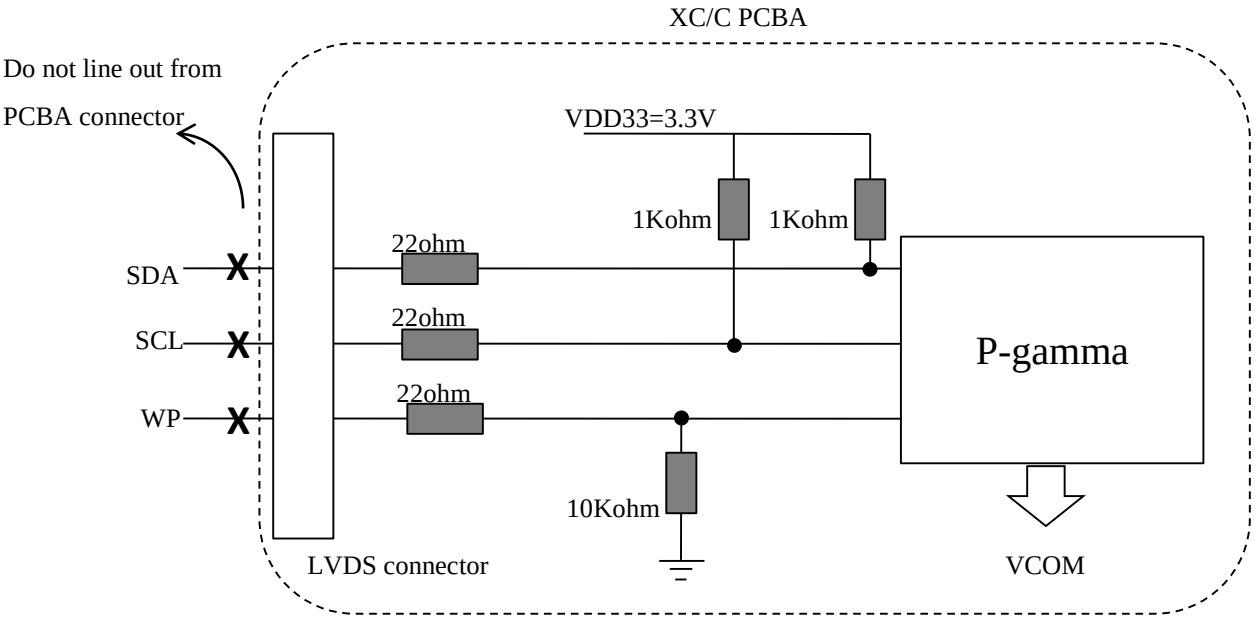


Fig. 4.2 WP/SDA/SCL PCBA set

b. For the VCOM (Flicker) regulation and control, SDA and SCL must pull high in the flicker set, and the flicker set's VDD must ready before the input power (VCC5V)

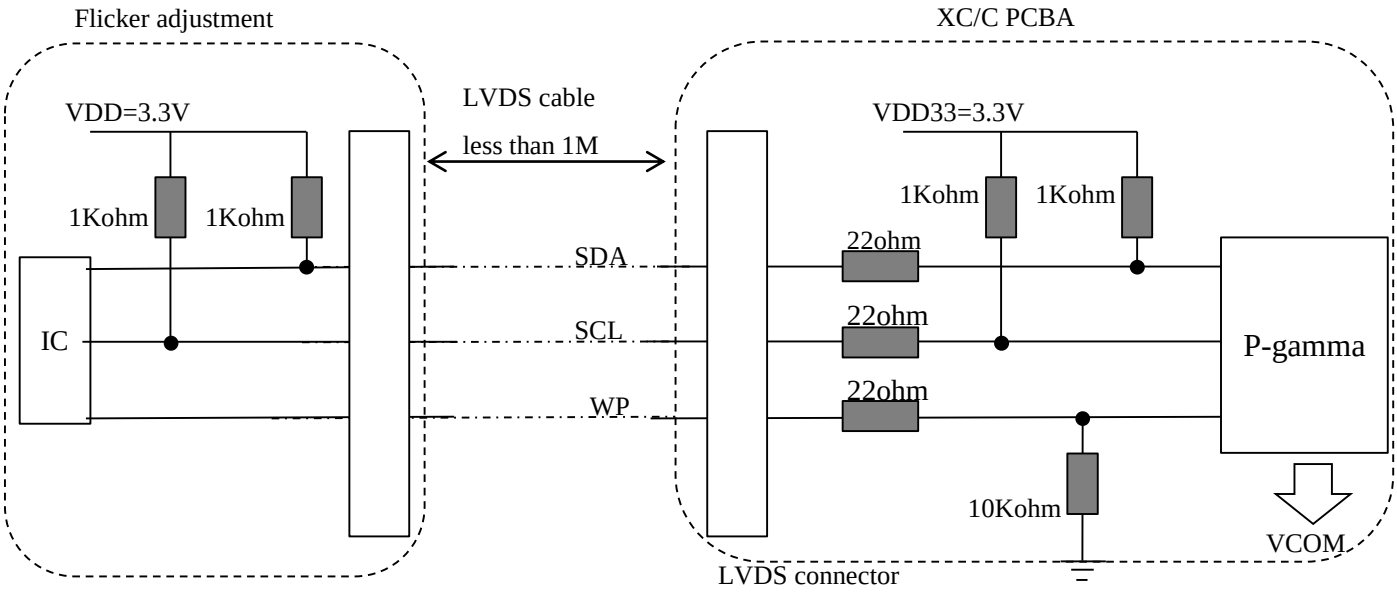


Fig. 4.3 WP/SDA/SCL flicker set

4.2 Block Diagram of Interface

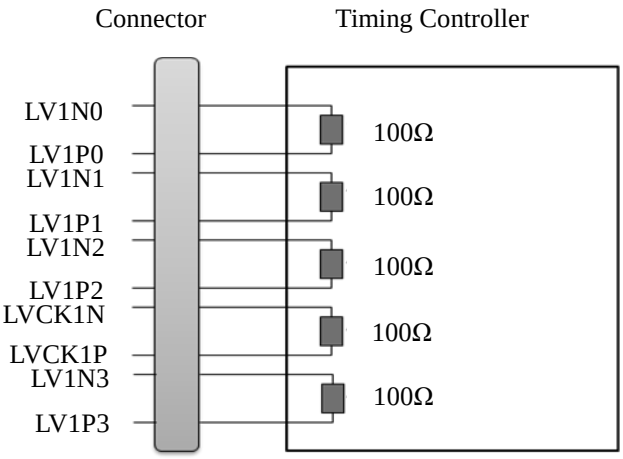


Fig. 4.4 Block diagram of interface

Attention:

(1) This open cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.

(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

4.3 LVDS Interface

4.3.1 VESA Format

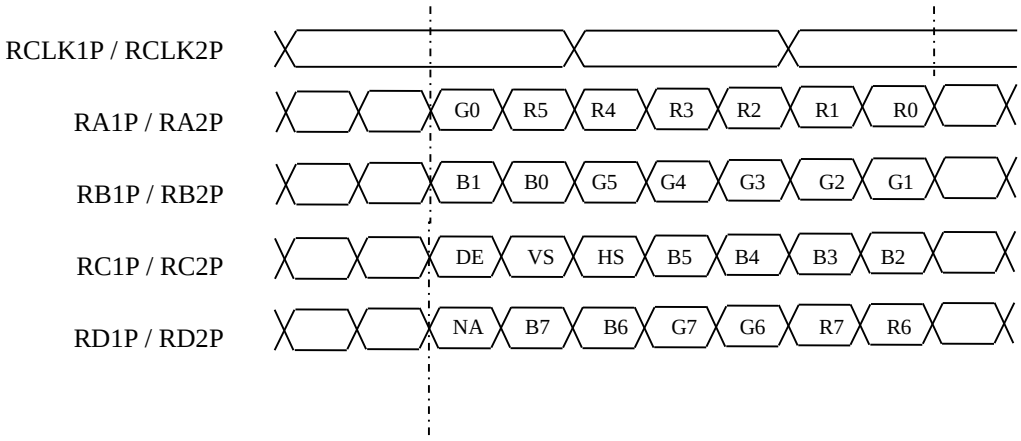


Fig. 4.5 VESA format

4.4 V-com Adjustment

(a) Flicker should be adjusted by optimizing the Vcom value in customer LCM line through the I2C interface.(Master & Slave = I2C communication)

Pin. NO.	Symbol	Function	Remark
1	WP	EN	Default:0V Vcom tunning:3.3V (Shouldn't be communicated with I2C device as output level "5V")
2	SCL_I	I2C Interface	I2C Interface
3	SDA_I	I2C Interface	

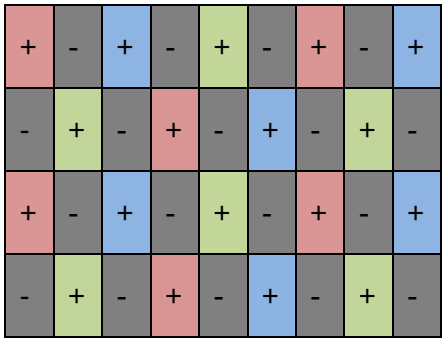
(b) Flicker should be tuned by correct method according to gamma IC type of each model.

Type	Flicker data saving position	Slave Address							
Genie Type	Gamma IC memory	B7	B6	B5	B4	B3	B2	B1	B0
		1	1	1	0	1	0	0	R/W-

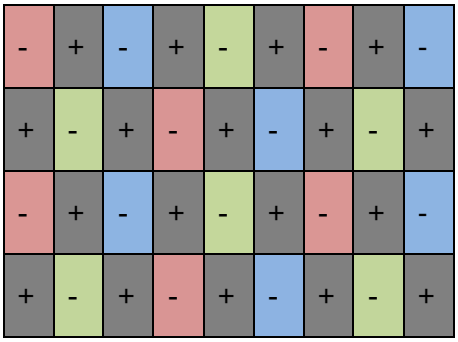
(c)Flicker Should be adjusted by the Dot on/off pattern

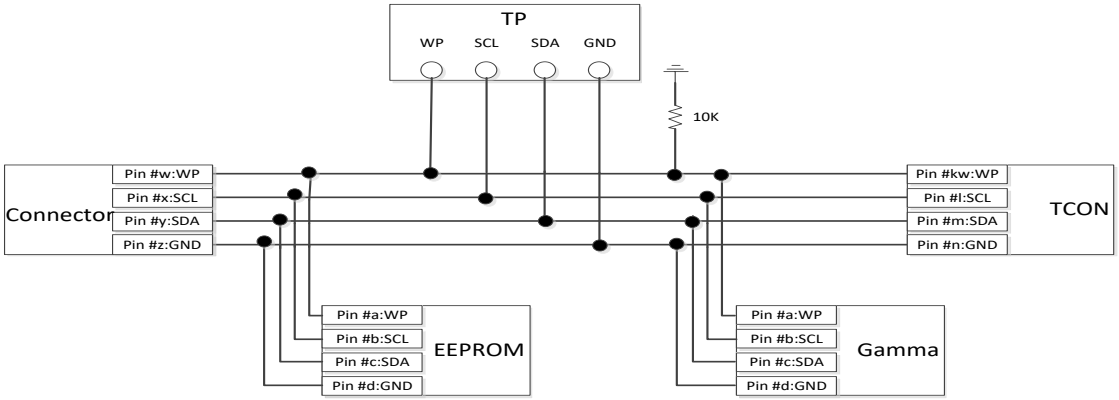
Dot on/off pattern

Frame N



Frame N+1





Flicker Adjust Circuit Block Diagram

5. Interface Timing

5.1 Timing Table (DE Only Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	Fclkin (=1/T_{Clk})	65	74.25	96	MHz	(1) (2)
	Input cycle to cycle jitter	Trcl	-	-	200	ps	(3)
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	-	Fclkin+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	60	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSM}	-400	-	400	ps	(5)
Vertical Active Display Term	Frame Rate	F	48	60	75	Hz	
	Total	T_V	1092	1125	1380	T_H	$T_V = T_{VD} + T_{VB}$
	Display	T_{VD}	1080				
	Blank	T_{VB}	12	45	300	T_H	
Horizontal Active Display Term	Total	T_H	1046	1100	1174	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Display	T_{HD}	960				
	Blank	T_{HB}	86	140	214	T_{CLK}	

Note:

(1) The TFT LCD open cell is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

(2) Please make sure the range of pixel clock follows the following equations:

Fclkin(max) ≥ Fmax × Tv × Th Fmin × Tv × Th ≥ Fclkin(min)

Main frequency Max is 96Mhz without spread spectrum

T_V

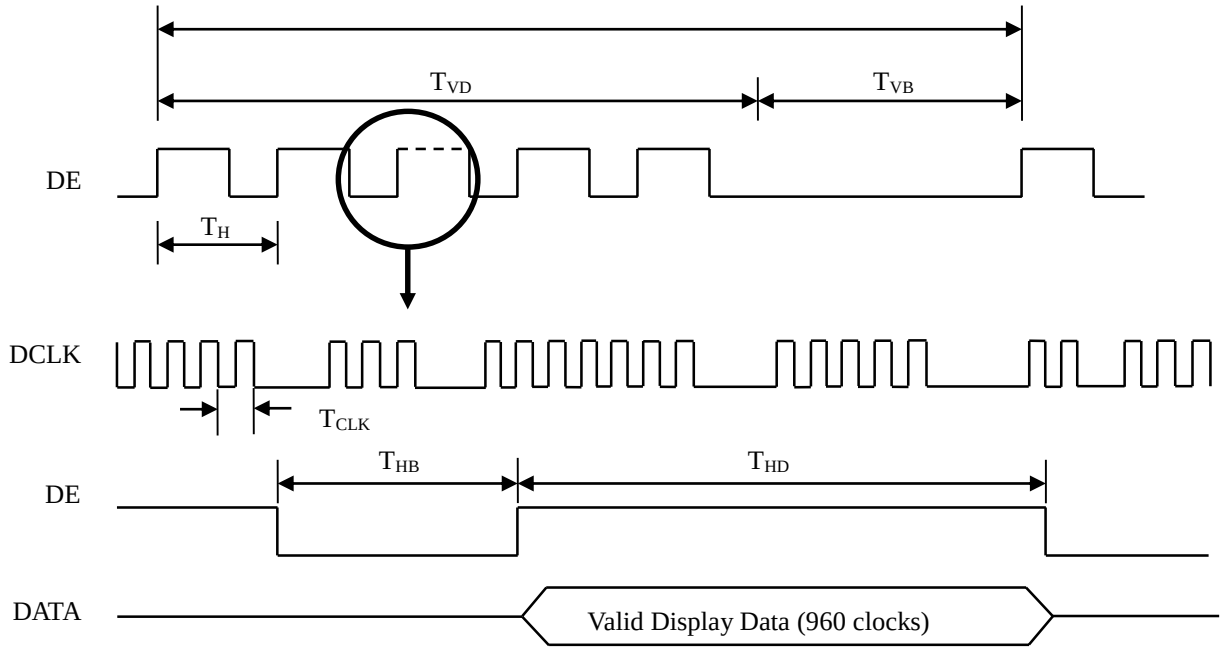


Fig. 5.1 Interface signal timing diagram

(3)The input clock cycle-to-cycle is defined as below figures.

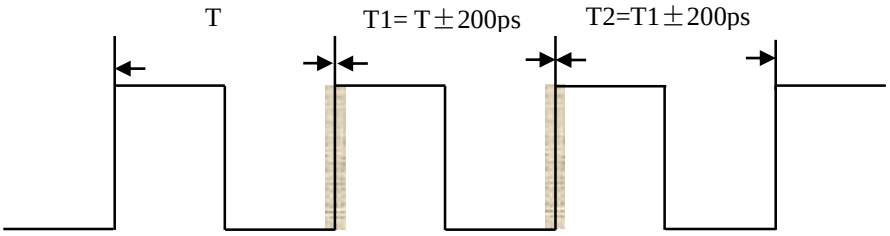


Fig. 5.2 Jitter

(4) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

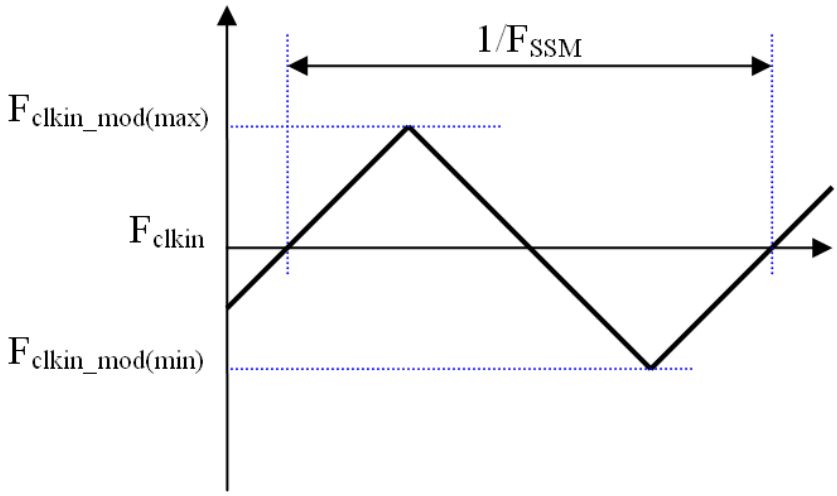


Fig. 5.3 SSCG

(5) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

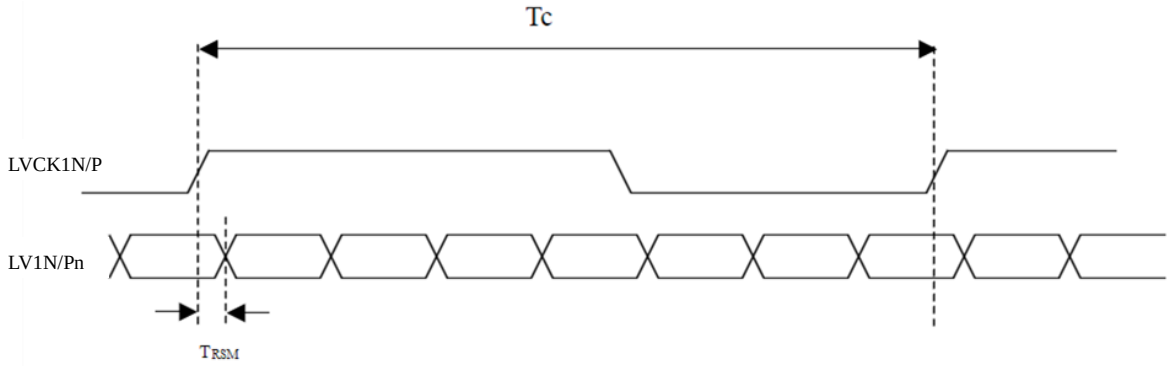


Fig.5.4 LVDS receive interface timing diagram

5.2 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.

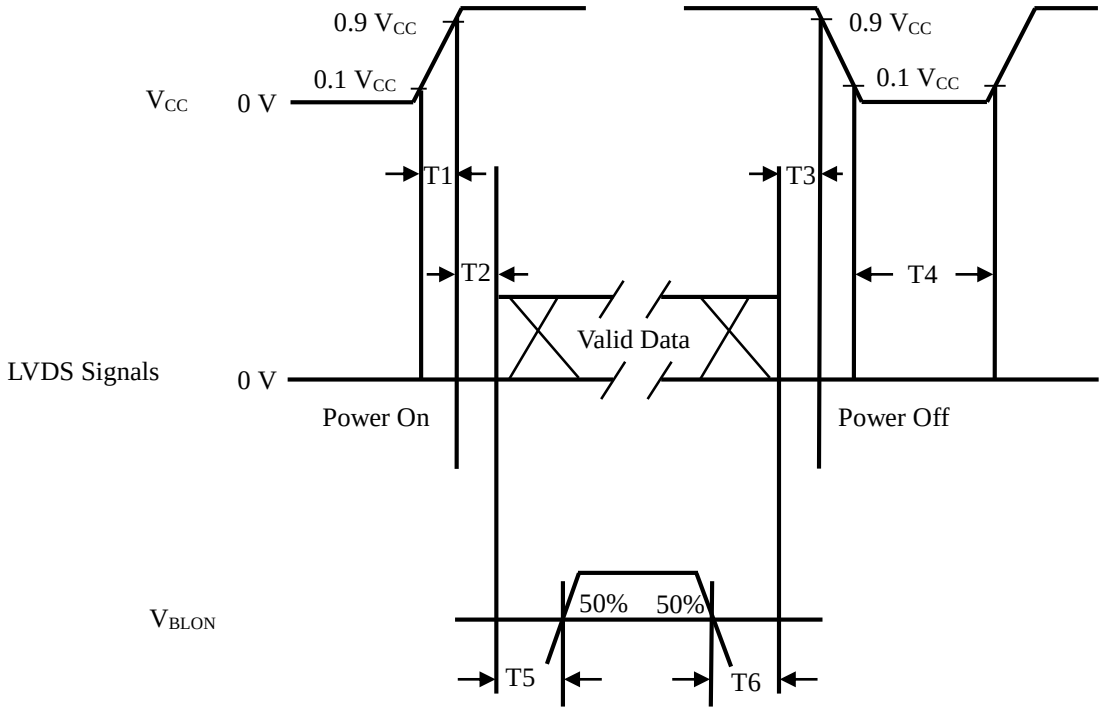


Fig.5.5 Power on/off sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	Min.
T1	0.5	-	10.0	ms
T2	0.0	-	50	ms
T3	0.0	-	50	ms
T4	1000.0	-	-	ms
T5	500.0	-	-	ms
T6	100.0	-	-	ms

Attention:

(1) The supply voltage of the external system for the open cell input should follow the definition of VCC.

(2) When the customer's backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case that VCC is in off level, please keep the level of input signals on the low or high impedance. If T2 < 0, that may cause electrical overstress.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

6. Optical Characteristics

6.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25 ± 2	℃
Ambient Humidity	H_A	50 ± 10	%RH
Supply Voltage	V_{CC}	5	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_R	60	Hz

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 60 minutes after lighting the backlight and in the windless environment.

To measure the LCD cell, it is suggested to set up the standard measurement system as Fig. 6.1. The measuring area S should contain at least 500 pixels of the LCD cell as illustrated in Fig.6.2 (A means the area allocated to one pixel). In this model, for example, the minimum measuring distance Z is 370mm when θ is 2 degree. Hence, 500mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

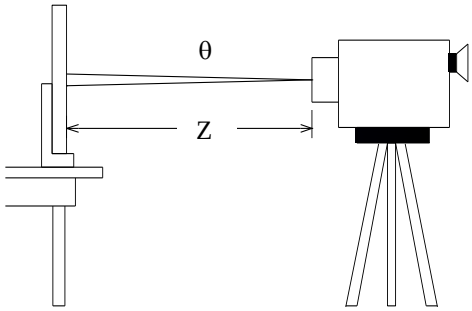


Fig. 6.1 The standard set-up system of measurement

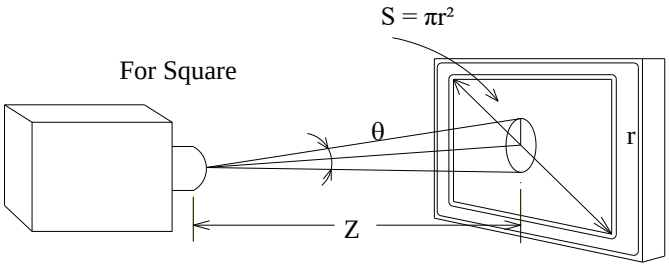


Fig. 6.2 The area S contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geqslant 500 \text{ pixels}$$

N means the actual number of the pixels in the area S.

6.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000, MINOLTA CA310, ELDIM OPTI Scope-SA and ELDIM EZ contrast in dark room.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR	$\theta_H = 0°$, $\theta_V = 0°$ Normal direction at center point of the LCD module.	-	4000	-	-	(1) (2)
Response Time		T_L		-	6.5	-	ms	(3) OPTI Scope-SA
Center Luminance		L_{W-2D}		900	1000	-	cd/m^2	(2) (4)
		L_{W-3D}		-	50	-	-	(5)
3D Crosstalk		CT-3D		-	3.5%	-	-	(5)
Uniformity of White Screen		-		75	-	-	%	(2) (6)
Color Chromaticity (CIE1931)	Red	R_X		Typ. - 0.03	0.639	Typ. + 0.03	-	(2) (7)
		R_Y			0.335		-	
	Green	G_X			0.319		-	
		G_Y			0.626		-	
	Blue	B_X			0.155		-	
		B_Y			0.052		-	
	White	W_X			0.280		-	
		W_Y			0.290		-	
	Color Gamut	CG		-	72	-	% NTSC	
Viewing Angle	Horizontal	θ_{H+}	CR ≥ 10	-	89	-	Deg.	(8) ELDIM EZ Contrast
		θ_{H-}		-	89	-		
	Vertical	θ_{V+}		-	89	-		
		θ_{V-}		-	89	-		

Note:

(1) Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\text{CR-W}}{\text{CR-D}}$$

CR-W is the luminance measured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 6.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black.

(2) The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000, (TOPCON) SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON)

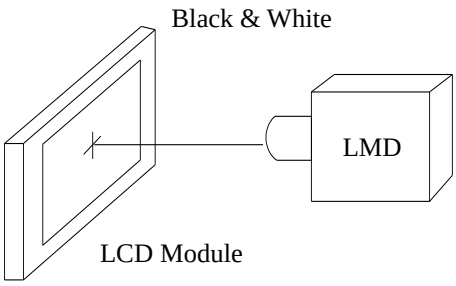


Fig. 6.3 The standard setup of CR measurement

(3) Response time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element $t_{X\ to\ Y}$ is the transition time from luminance ratio X to Y. X and Y are two different luminance ratios among 0%, 25%, 50%, 75%, and 100% luminance. The transition time $t_{X\ to\ Y}$ is defined as the time taken from 10% to 90% of the luminance difference between X and Y (X < Y) as illustrated in Fig.6.4. When X > Y, the definition of $t_{X\ to\ Y}$ is the time taken from 90% to 10% of the luminance difference between X and Y. The response time is optimized on refresh rate F_r = 60Hz.

Measured Transition Time		Luminance Ratio of Previous Frame				
		0%	25%	50%	75%	100%
Luminance Ratio of Current Frame	0%		$t_{25\%\ to\ 0\%}$	$t_{50\%\ to\ 0\%}$	$t_{75\%\ to\ 0\%}$	$t_{100\%\ to\ 0\%}$
	25%	$t_{0\%\ to\ 25\%}$		$t_{50\%\ to\ 25\%}$	$t_{75\%\ to\ 25\%}$	$t_{100\%\ to\ 25\%}$
	50%	$t_{0\%\ to\ 50\%}$	$t_{25\%\ to\ 50\%}$		$t_{75\%\ to\ 50\%}$	$t_{100\%\ to\ 50\%}$
	75%	$t_{0\%\ to\ 75\%}$	$t_{25\%\ to\ 75\%}$	$t_{50\%\ to\ 75\%}$		$t_{100\%\ to\ 75\%}$
	100%	$t_{0\%\ to\ 100\%}$	$t_{25\%\ to\ 100\%}$	$t_{50\%\ to\ 100\%}$	$t_{75\%\ to\ 100\%}$	

$t_{X\ to\ Y}$ means the transition time from luminance ratio X to Y.

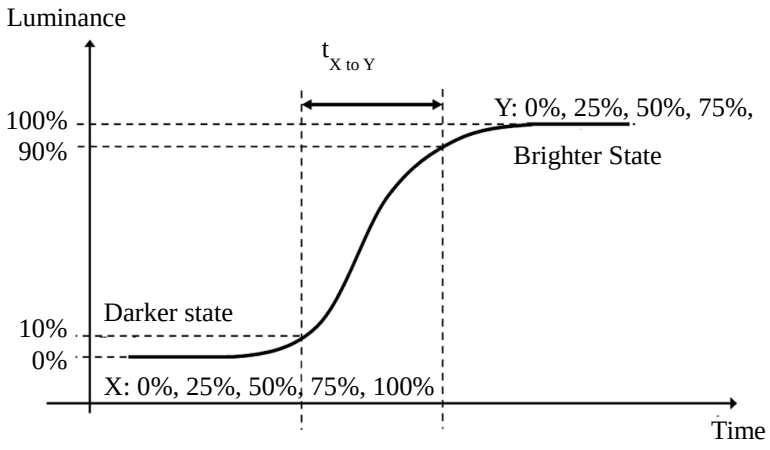


Fig. 6.4 The definition of $t_{X\ to\ Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

(4) Definition of center Transmittance (T %):

The transmittance is measured with full white pattern (Gray 255)

$$\text{Center Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(5) Definition of the crosstalk(CT-2D):

YA = Luminance of measured location without gray level 255 pattern (cd/m^2)

YB = Luminance of measured location with gray level 255 pattern(cd/m^2)

Definition of the crosstalk: $CT = \frac{YB-YA}{YA}$

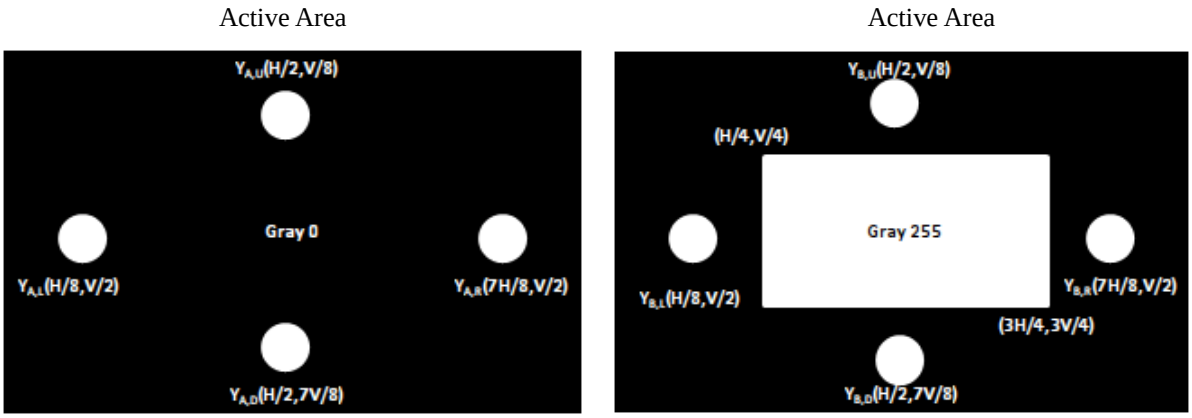


Fig. 6.5 The definition of 2D mode crosstalk

(6) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1931 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 6.6.

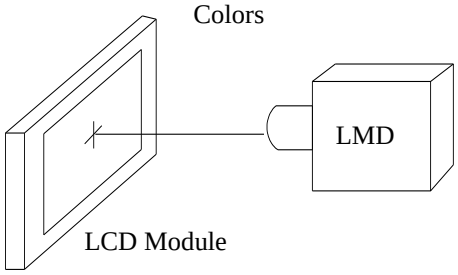


Fig. 6.6 The standard setup of color chromaticity measurement

(7) Definition of viewing angle coordinate system (θ_H, θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module (two vertical angles: up θ_{V+} and down θ_{V-}; and two horizontal angles: right θ_{H+} and left θ_{H-}) as illustrated in Fig. 6.7. The contrast ratio is measured by ELDIM EZ Contrast.

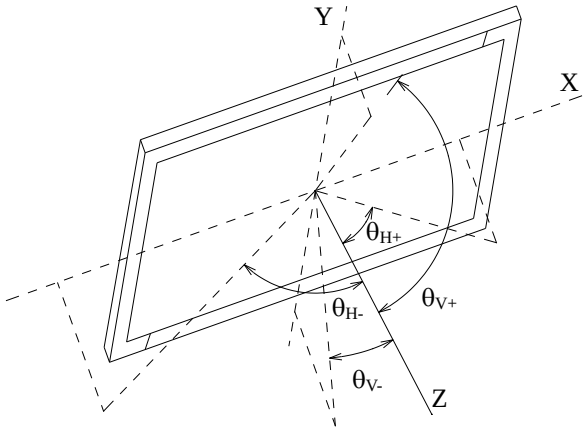
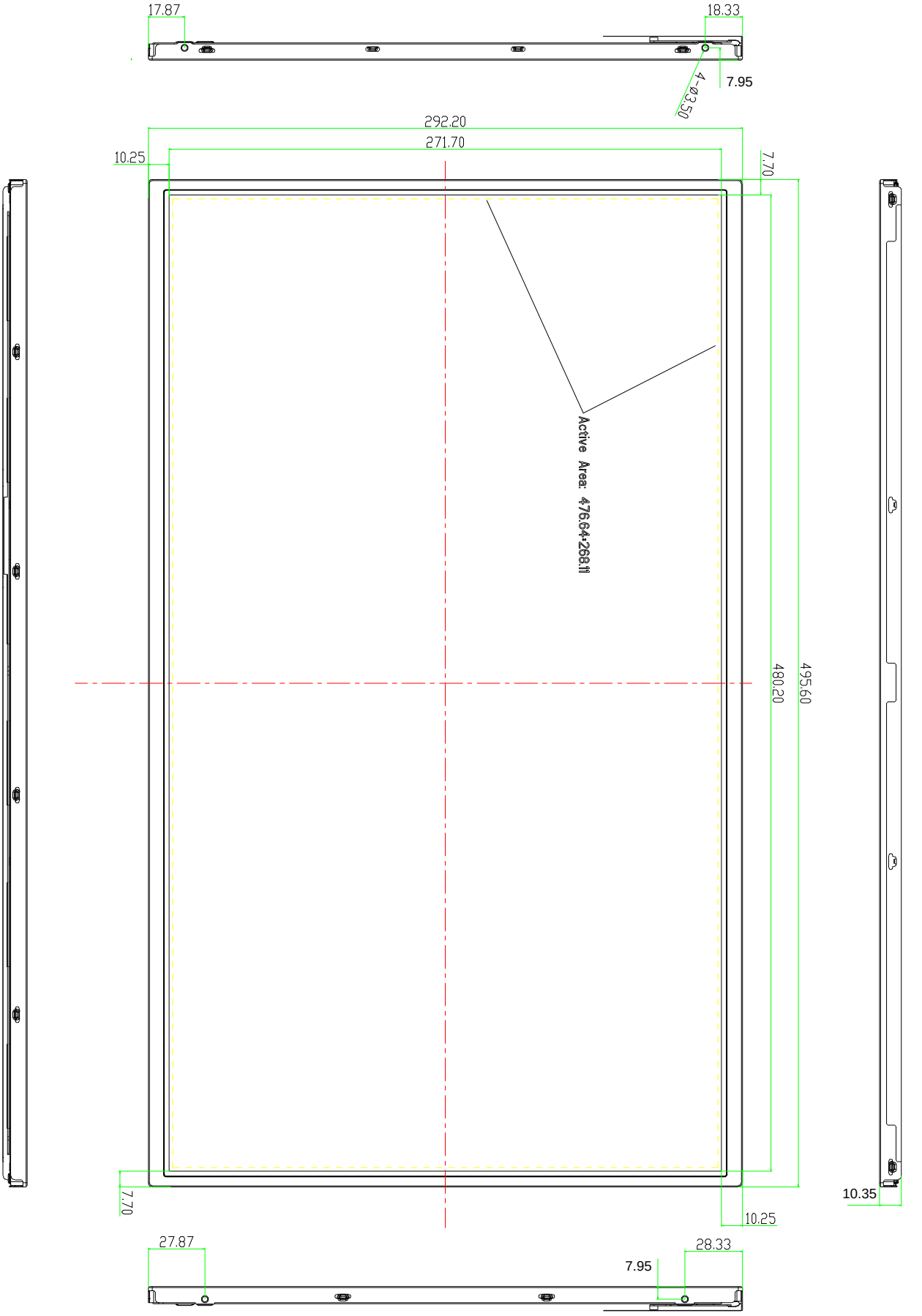
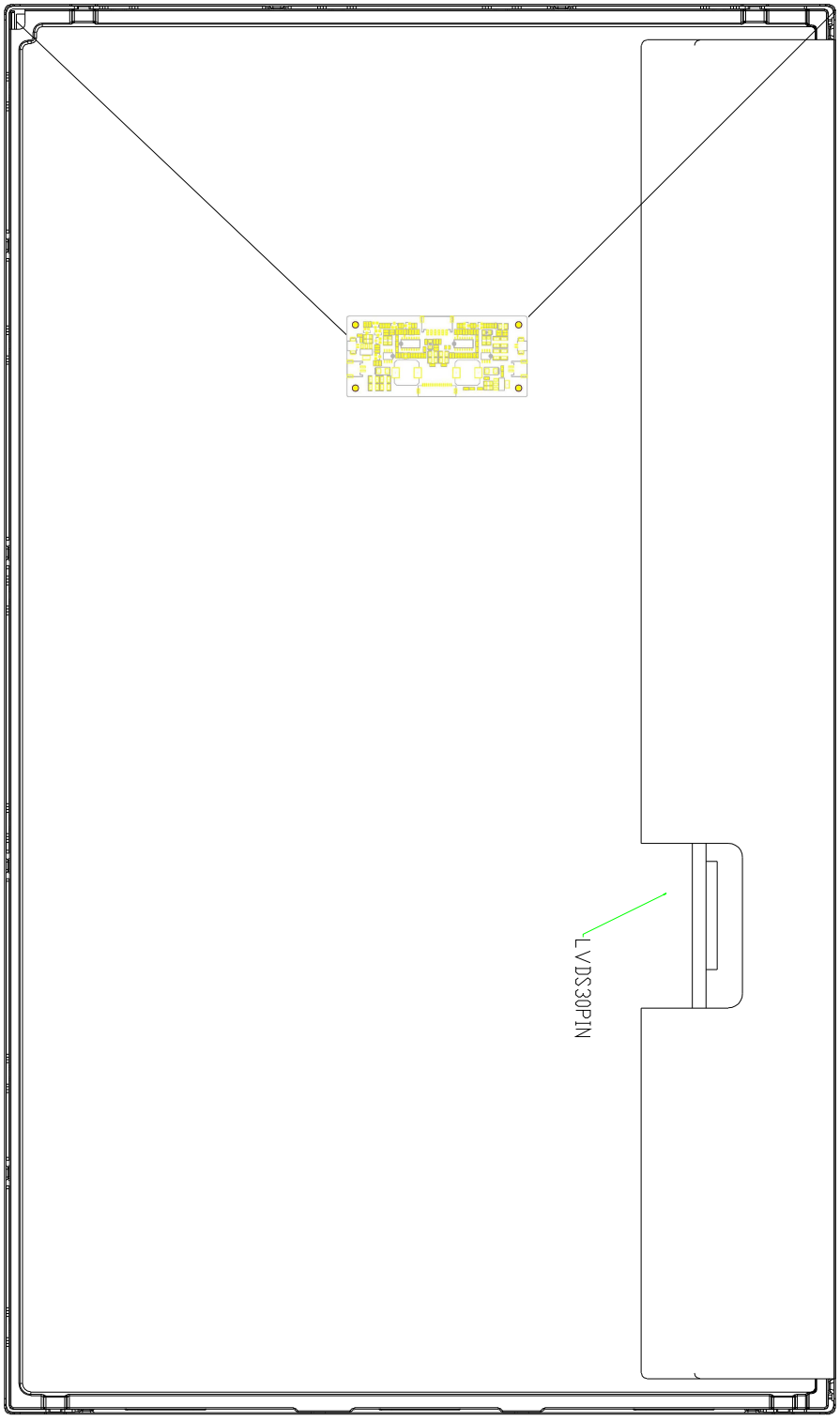


Fig. 6.7 Viewing angle coordination system

7. Mechanical Characteristics

7.1 Measurement Conditions




LVDS30PIN